Total Verification System
User's Manual

Notice of Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Ingenion products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Ingenion hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Ingenion shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Ingenion had been advised of the possibility of the same. Ingenion assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties; IP cores may be subject to warranty and support terms contained in a license issued to you by Ingenion. Unless otherwise stated, Ingenion products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Ingenion products in Critical Applications.

Revision History

Date	Version	Description
9/24/3017		Updated figure 3-1

Contents

1 Concept 5
1.1 Simulation 5
1.2 Board Testing 6
1.3 Box Integration and Testing 7
1.4 Flight Software Acceptance Testing 8
1.5 Common Elements 9
1.5.1 Hardware 9
1.5.2 Software 10
2 Block Diagram 11
3 Hardware Interfaces 11
3.1 RS-422 13
3.1.1 RS-422 Connectors – J1 to J4 13
3.2 UART 17
3.2.1 UART Connectors – J5 17
3.3 SpaceWire 18
3.3.1 SpaceWire Connectors – J6 to J11 18
3.3.2 Link Margin Testing 20
3.4 TTL Input/Output 21
3.4.1 xTTL Output Connector – J12 22
3.4.2 xTTL Input Connector – J13 24
3.5 Opal Kelly XEM3010 25
3.5.1 Board to Board Connector – J100, J101 25
3.5.2 Configuration 27
3.6 Opal Kelly XEM6310 28
3.6.1 Board to Board Connector – JP1, JP2 28
3.7 Opal Kelly XEM7310 30
3.7.1 Board to Board Connector – MC1, MC2 30
3.8 Power 32
3.8.1 USB Power for XEM Boards 32
3.8.2 External Power – J15 32

3.8.3 External Power – J16 33
4. Appendix A - Loopback Plugs 34
4.1 LP1 34
4.2 LP2 35
4.3 LP3 35
4.4 LP4 36
4.5 LC5 37
5. Appendix B - FPGA Pinout Attachments 37

1 Concept

This section explains a generic board and FPGA verification process that spans simulation, board testing, box testing, and flight software acceptance testing. The goal for this testing concept is to reduce cost and schedule while improving the quality, integrity, and reliability of the testbench. This is accomplished by identifying common hardware and software elements throughout the end-to-end design and verification process and planning, early on, to implement and reuse the common resources.

1.1 Simulation

Simulation programs and personal computers have become powerful enough that board level simulations of designs that contain multiple FPGAs are now feasible. The plan for code 561.0 is to perform board-level simulations for all cards and resort to FPGA-level simulations only for FPGA designs which are mission-independent and which have many corner cases that cannot be created in board-level simulation.

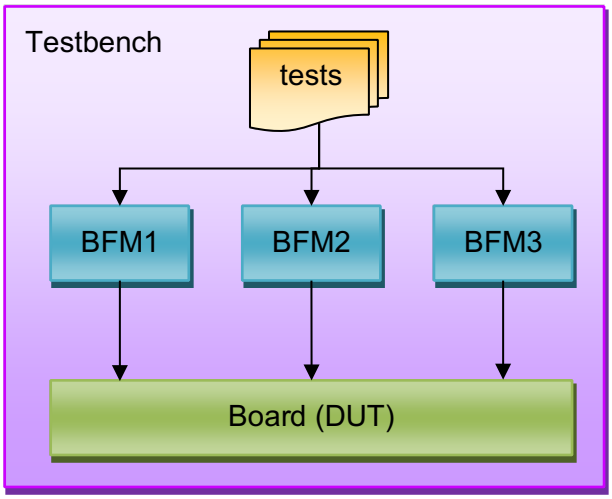


Figure 1-1 Board-Level Simulation Testbench

The board-level simulation shall implement a suite of tests that are automated and self-checking. Each test shall verify one or more requirements or features of the board. The combined suite of tests shall verify all the derived board-level requirements and features found in the specification. The tests shall be planned and explained in detail in the board verification plan.

To assist in the simulation, bus functional models, BFMs are used to exercise all the interfaces of the DUT. Some interfaces are digital, other are analog. The BFMs are controlled by the test and capture information that is read by the test and used to determine proper behavior of the DUT. The BFMs should be as rudimentary as possible, leaving all data generation and validation to the test.

The device under test, DUT, can contain FPGAs, discrete digital components, and analog components. All components on the board shall be modeled in simulation. For FPGAs, the actual RTL code shall be used. For discrete digital components, behavioral HDL can be used to model the devices.

For analog components in the DUT or BFMs, a Spice model can be used if a simulator that supports mixed mode analog and digital simulation is used. For code 561.0, Modelsim is the planned simulator so the function of analog circuits will be coarsely modeled with behavioral VHDL using floating point signals and variables.

The testbench glues together all the elements of simulation. It performs tasks such as compiling code, running processes, logging information, generating reports, and running multiple tests in an automated fashion.

1.2 Board Testing

Board testing is performed with actual hardware once the DUT has been fabricated and assembled. Board testing requires GSE for driving DUT inputs and sampling DUT outputs. Board testing is the process of verifying that the DUT contains no manufacturing flaws and meets all the board-level requirements and specified card features. Board testing is different from design debugging which mostly occurs after the assembly of the first revision of the DUT. Design debugging preempts board testing and occurs when a board test fails. Board testing can be performed by a test conductor following a test plan on successive iterations of the DUT.

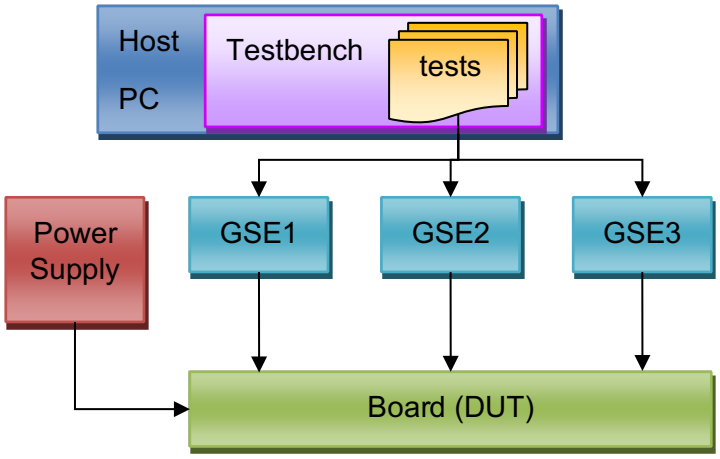


Figure 1-2 Board-Level Lab Testbench

The board-level lab test bench shall implement a suite of tests that are automated and self-checking. Each test shall verify one or more requirements or features of the board. The combined suite of tests shall verify all the derived board-level requirements and features found in the specification. The tests shall be planned and explained in detail in the board verification plan.

To assist in the lab testing, ground support equipment, GSE, components are used to exercise all the interfaces of the DUT. Some interfaces are digital, other are analog. The GSE components are controlled by the test and capture information that is read by the test and used to determine proper behavior of the DUT. Some GSE components are COTS equipment like 1553 cards, while other GSE components are custom built by GSFC.

The test bench glues together all the elements of lab testing. It performs tasks such as compiling code, running processes, logging information, generating reports, and running multiple tests in an automated fashion.

1.3 Box Integration and Testing

After each card is tested, it must be integrated into the box and tested. This environment requires the use of GSE that is controlled by a host terminal. The tests should be self-checking and automated. The following diagram shows how box level testing is implemented.

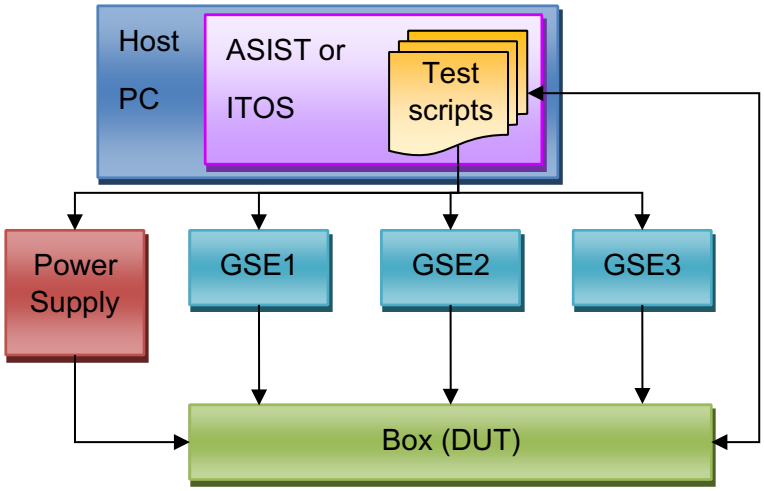


Figure 1-3 Box-Level Lab Testbench

The box-level lab testbench shall implement a suite of tests that are automated and self-checking. Each test shall verify one or more box level requirement or features of the box. The combined suite of tests shall verify all the derived box-level requirements and features found in the box specification. The tests shall be planned and explained in detail in the box verification plan.

To assist in the lab testing, ground support equipment, GSE, components are used to exercise all the interfaces of the DUT. Many of the GSE components used in box level testing are the same as those used in board-level testing. The GSE components are controlled by the test and capture information that is read by the test and used to determine proper behavior of the DUT.

The ASIST environment glues together all the elements of testing. It performs tasks such as running scripts, logging information, generating reports, and running multiple scripts in an automated fashion.

1.4 Flight Software Acceptance Testing

When all the cards of the box have been integrated and the box hardware has been tested, the Goddard dynamic simulator, GDS, is used to validate the final build of flight software. The GDS emulates the dynamic behavior of the GNC sensors and actuators as if the spacecraft were actually in flight. The following diagram shows the flight software acceptance testbench.

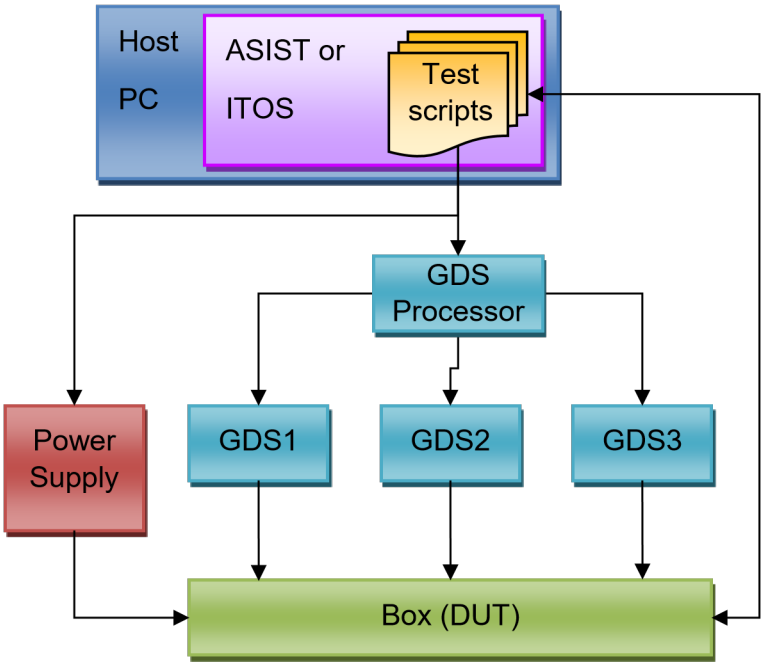


Figure 1-4 Flight Software Acceptance Testbench

The flight software acceptance testbench shall implement a suite of tests that are automated and self-checking. Each test shall verify one or more software requirement or features of the flight software. The combined suite of tests shall verify all the derived flight software requirements and features found in the software specification. The tests shall be planned and explained in detail in the flight software verification plan.

To assist in the software testing, GDS, components are used to exercise all the interfaces of the DUT.

Many of the GDS components used in software testing are the same as those used in box-level testing. The configuration of the GDS is controlled by the test. The GDS single board computer controls the dynamic behavior of the interfaces to the DUT. The test scripts capture information that is generated by the DUT and used to determine proper behavior of the DUT.

The ASIST or ITOS environment glues together all the elements of testing. It performs tasks such as running scripts, logging information, generating reports, and running multiple scripts in an automated fashion.

1.5 Common Elements

This section analyzes the common elements of the design and verification phases from a board-level perspective. Thus, common elements between box level and software testing are not identified.

1.5.1 Hardware

Refer to the Figure 1-1 to Figure 1-4 for this section.

1.5.1.1 Bus Functional Models

The BFMs used in board level simulation should be designed to mirror the capabilities of the GSE hardware used in board, box, and software testing. For COTS or existing GSE, the BFM should be designed against the user manual for the GSE or COTS equipment. Examples of this are the 1553 BC card or GDS thruster emulation boards. For new custom designs such as the SComm to PSE interface, the GSE design should be planned first then the BFM.

1.5.1.2 New Custom Ground Support Equipment

New custom GSE should be designed using a platform that can be quickly and easily used in the simulation environment. For example, Opal Kelly makes a programmable USB board that contains a Xilinx Spartan FPGA that can be used to contain the same BFM code used in simulation. A daughter card can be designed that interfaces to the Xilinx FPGA IO pins and to the DUT. In simulation the BFM and components on the daughter card are simulated and are controlled by the test in the same way as during board-level testing. See the diagram below to see how this is accomplished.

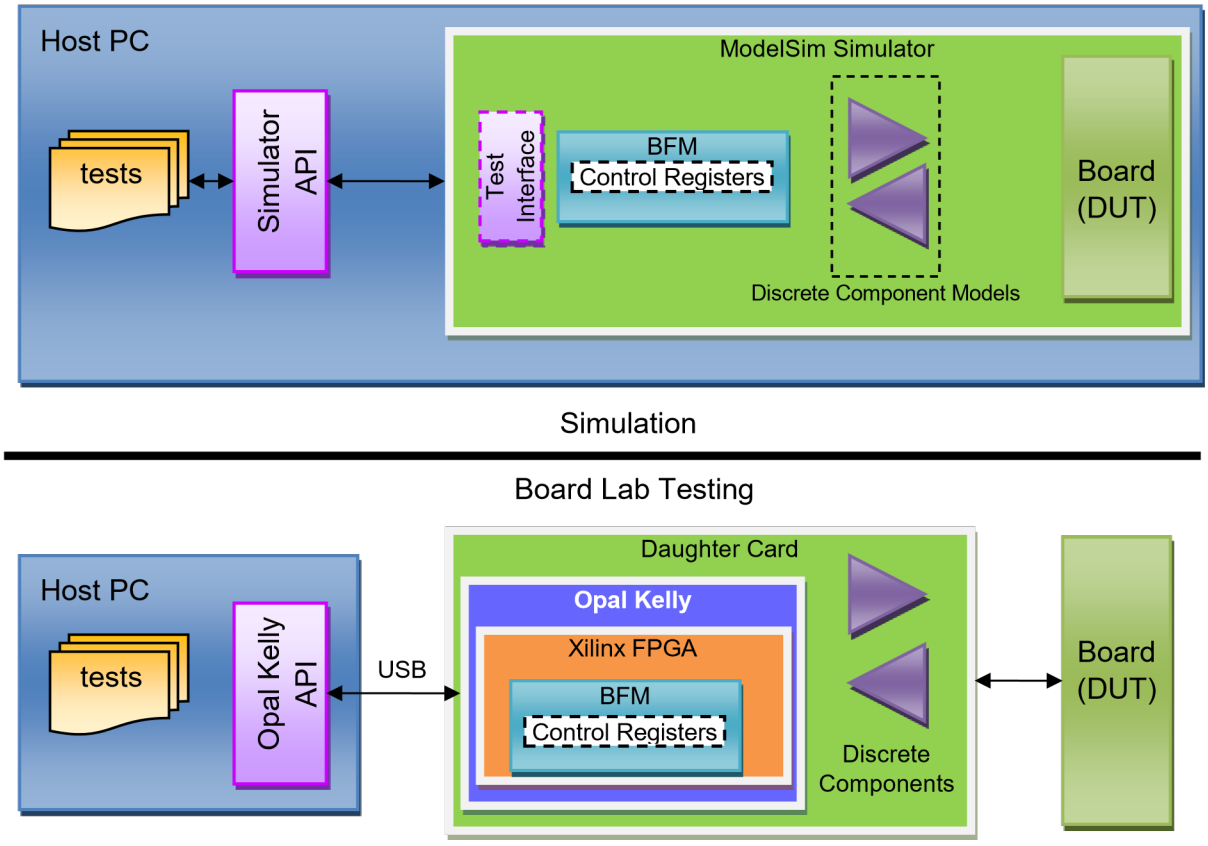


Figure 1-5 New Custom GSE/BFM Using Opal Kelly Platform

1.5.2 Software

1.5.2.1 Simulation and Board-level Tests

The tests written in the simulation phase can be used in lab testing with very little, if any, modification. To accomplish this task, the tests should be written in a language that can port over from simulation to lab testing. For code 561.0, C++ will be used. An abstraction layer of software which contains the Opal Kelly API and the Simulator API allows tests to be compiled so that they communicate with either the simulator or the GSE depending on the testing environment.

1.5.2.2 Board-level and Box-level Classes

In developing the C++ tests, the verification engineer should plan out the classes of code needed to implement the test. Some classes, which are used in simulation and board testing, will be portable to box level testing as well. These classes can be compiled into the box-level scripting environment and made available to box-level test scripts. An example of this would be a class used by DIO board-level testing to control the GPS BFM which emulates a GPS receiver.

2 Block Diagram

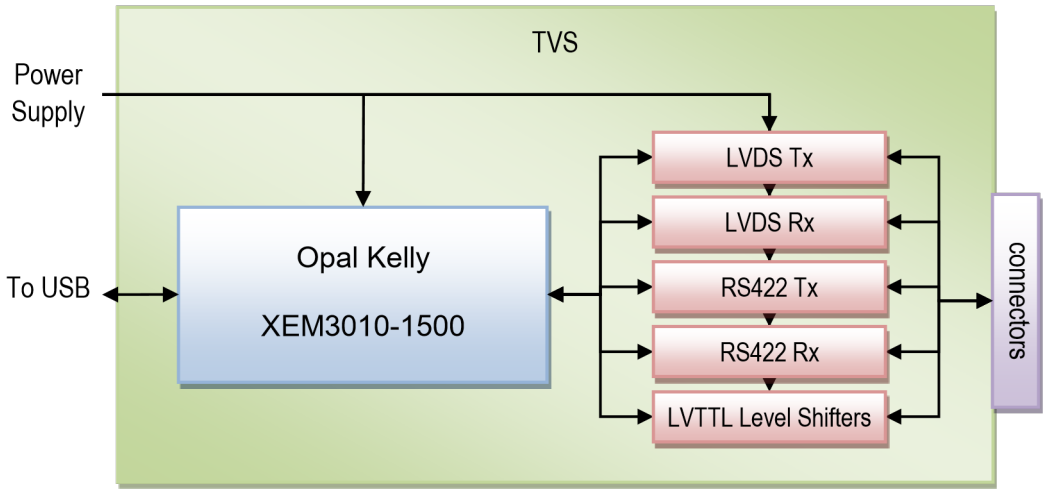


Figure 2-1 – TVS Assembly Block Diagram

3 Hardware Interfaces

This section describes the connector interfaces of the TVS card in detail. The following table lists all the resources provided by the TVS card in its default configuration (unmodified).

Table 3-1 TVS Resources

Resource	Quantity
SpaceWire Connectors	6
SpaceWire Links	4
UART[4] ports	4
Single-Ended Inputs (3.3-15V) [3]	8
TTL or LVTTL[2] Outputs	20
RS-422 Inputs[1]	40
RS-422 Outputs[1]	16

1. Can be replaced with LVDS in groups of 4
2. Jumper configurable in groups of 4
3. Higher voltages are possible when making use of the built-in voltage divider network.
4. Each UART composes of one RS422 pair for Tx and one for Rx.

The following diagram shows the connectors on the TVS enclosure's front and rear panels.
NOTE: J16 and J14 locations will vary with TVS model.

Front

Back

Figure 3-1 – TVS Connector Diagram

3.1 RS-422

J1 to J4 provide RS-422 inputs and outputs using Texas Instruments AM26LV31INSR transmitters and Texas Instruments AM26LV32IDR receivers. These parts are pin-for-pin compatible with LVDS drivers/receivers which can be used to provide additional LVDS IO. All RS-422 input signals are terminated with 100 ohm shunt resistors rated for 100mW. All RS-422 output signals are terminated with two 45 ohm series resistors rated for 63mW each. These termination resistors may be removed or replaced with zero-ohm resistors as needed. Note that if RS-422 drivers are replaced with LVDS drivers, the 45ohm series termination resistors should be replaced with 0-ohm resistors.

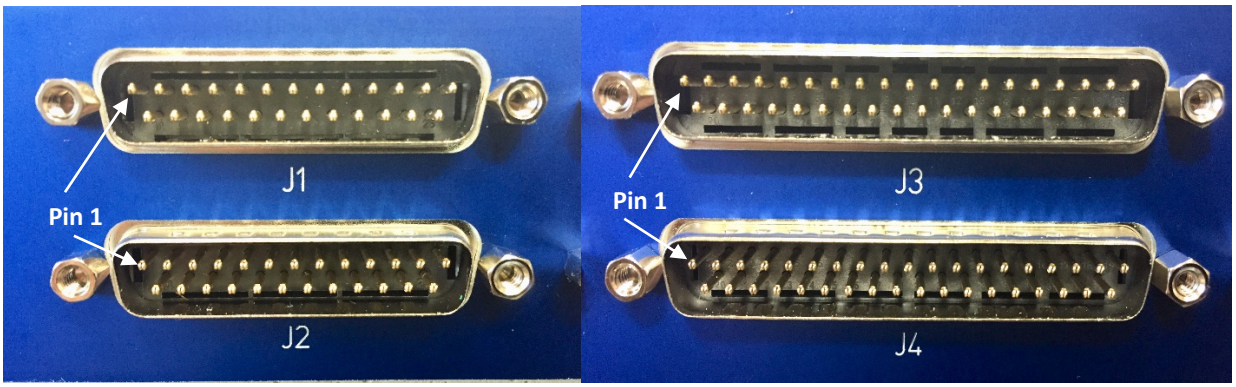


Figure 3-2 – J1 to J4

3.1.1 RS-422 Connectors – J1 to J4

The pinout for J1 and J2 is identical, except for the signals in red, and are shown in the table below. Both are 25-pin low density D-sub male connectors. Signals in

Table 3-2 RS-422 IO Connector – J1, J2 Sorted by Pin Number

Connector Pin	Signal J1	Signal J2
1	RS422_In_1_N	RS422_In_10_N
2	RS422_In_2_N	RS422_In_9_N
3	RS422_In_3_P	RS422_In_11_P
4	RS422_In_0_N	RS422_In_8_P
5	RS422_In_5_P	RS422_In_14_N
6	RS422_In_6_N	RS422_In_13_N
7	RS422_In_7_P	RS422_In_15_P
8	RS422_In_4_N	RS422_In_12_P
9	RS422_Out_2_P	RS422_Out_1_P
10	RS422_Out_2_N	RS422_Out_1_N
11	RS422_Out_3_N	RS422_Out_0_N
12	RS422_Out_3_P	RS422_Out_0_P

13	RS422_Out_6_P	RS422_Out_5_P
14	RS422_In_1_P	RS422_In_10_P
15	RS422_In_2_P	RS422_In_9_P
16	RS422_In_3_N	RS422_In_11_N
17	RS422_In_0_P	RS422_In_8_N
18	RS422_In_5_N	RS422_In_14_P
19	RS422_In_6_P	RS422_In_13_P
20	RS422_In_7_N	RS422_In_15_N
21	RS422_In_4_P	RS422_In_12_N
22	RS422_Shield	RS422_Shield
23	RS422_Shield	RS422_Shield
24	RS422_Shield	RS422_Shield
25	RS422_Out_6_N	RS422_Out_5_N

** Unlisted connector pins are no connects*

3-3 422 IO Connector J1, J2 Sorted by Signal Name

Connector Pin	Signal J1	Term. RefDes	Signal J2	Term. RefDes
4	RS422_In_0_N	R609	RS422_In_8_P	R625
17	RS422_In_0_P		RS422_In_8_N	
1	RS422_In_1_N	R610	RS422_In_10_N	R626
14	RS422_In_1_P		RS422_In_10_P	
2	RS422_In_2_N	R613	RS422_In_9_N	R629
15	RS422_In_2_P		RS422_In_9_P	
16	RS422_In_3_N	R614	RS422_In_11_N	R630
3	RS422_In_3_P		RS422_In_11_P	
8	RS422_In_4_N	R617	RS422_In_12_P	R633
21	RS422_In_4_P		RS422_In_12_N	
18	RS422_In_5_N	R618	RS422_In_14_P	R634
5	RS422_In_5_P		RS422_In_14_N	
6	RS422_In_6_N	R621	RS422_In_13_N	R637
19	RS422_In_6_P		RS422_In_13_P	
20	RS422_In_7_N	R622	RS422_In_15_N	R638
7	RS422_In_7_P		RS422_In_15_P	
10	RS422_Out_2_N	R608	RS422_Out_1_N	R606
9	RS422_Out_2_P	R607	RS422_Out_1_P	R605
11	RS422_Out_3_N	R652	RS422_Out_0_N	R604
12	RS422_Out_3_P	R651	RS422_Out_0_P	R603
25	RS422_Out_6_N	R649	RS422_Out_5_N	R647
13	RS422_Out_6_P	R648	RS422_Out_5_P	R646
22	RS422_Shield	NA	RS422_Shield	NA
23	RS422_Shield	NA	RS422_Shield	NA
24	RS422_Shield	NA	RS422_Shield	NA

The pinout for J3 and J4 is identical, expect for the signals in red, and are shown in the table below. Both are 37-pin low density D-sub male connectors.

3-4 422 IO Connector J3, J4 Sorted by Pin Number

Connector Pin	Signal J3	Signal J4
1	RS422_Out_7_P	RS422_Out_4_P
2	RS422_Shield	RS422_Shield
3	RS422_Out_9_P	RS422_Out_14_P
4	RS422_Out_10_N	RS422_Out_13_N
5	RS422_Out_11_N	RS422_Out_15_N
6	RS422_Shield	RS422_Shield
7	RS422_Out_8_N	RS422_Out_12_P
8	RS422_In_17_N	RS422_In_25_N
9	RS422_In_18_P	RS422_In_26_N
10	RS422_In_19_N	RS422_In_21_N
11	RS422_In_16_P	RS422_In_22_N
12	RS422_In_29_N	RS422_In_20_P
13	RS422_In_30_P	RS422_In_23_P
14	RS422_In_31_N	RS422_In_27_P
15	RS422_In_28_P	RS422_In_24_N
16	RS422_In_38_P	RS422_In_39_P
17	RS422_In_37_N	RS422_In_32_N
18	RS422_In_34_N	RS422_In_35_N
19	RS422_In_33_N	RS422_In_36_P
20	RS422_Out_7_N	RS422_Out_4_N
21	RS422_Out_9_N	RS422_Out_14_N
22	RS422_Out_10_P	RS422_Out_13_P
23	RS422_Shield	RS422_Shield
24	RS422_Out_11_P	RS422_Out_15_P
25	RS422_Out_8_P	RS422_Out_12_N
26	RS422_In_17_P	RS422_In_25_P
27	RS422_In_18_N	RS422_In_26_P
28	RS422_In_19_P	RS422_In_21_P
29	RS422_In_16_N	RS422_In_22_P
30	RS422_In_29_P	RS422_In_20_N
31	RS422_In_30_N	RS422_In_23_N
32	RS422_In_31_P	RS422_In_27_N
33	RS422_In_28_N	RS422_In_24_P
34	RS422_In_38_N	RS422_In_39_N
35	RS422_In_37_P	RS422_In_32_P
36	RS422_In_34_P	RS422_In_35_P

37	RS422_In_33_P	RS422_In_36_N

** Unlisted connector pins are no connects*

3-5 422 IO Connector J3, J4 Sorted by Signal Name

Connector Pin	Signal J3	Term. RefDes	Signal J4	Term. RefDes
29	RS422_In_16_N	R732	RS422_In_22_P	R704
11	RS422_In_16_P		RS422_In_22_N	
8	RS422_In_17_N	R733	RS422_In_25_N	R709
26	RS422_In_17_P		RS422_In_25_P	
27	RS422_In_18_N	R736	RS422_In_26_P	R712
9	RS422_In_18_P		RS422_In_26_N	
10	RS422_In_19_N	R737	RS422_In_21_N	R701
28	RS422_In_19_P		RS422_In_21_P	
33	RS422_In_28_N	R716	RS422_In_24_P	R708
15	RS422_In_28_P		RS422_In_24_N	
12	RS422_In_29_N	R717	RS422_In_20_P	R700
30	RS422_In_29_P		RS422_In_20_N	
31	RS422_In_30_N	R720	RS422_In_23_N	R705
13	RS422_In_30_P		RS422_In_23_P	
14	RS422_In_31_N	R721	RS422_In_27_P	R713
32	RS422_In_31_P		RS422_In_27_N	
19	RS422_In_33_N	R725	RS422_In_36_P	R740
37	RS422_In_33_P		RS422_In_36_N	
18	RS422_In_34_N	R728	RS422_In_35_N	R729
36	RS422_In_34_P		RS422_In_35_P	
17	RS422_In_37_N	R741	RS422_In_32_N	R724
35	RS422_In_37_P		RS422_In_32_P	
34	RS422_In_38_N	R744	RS422_In_39_N	R745
16	RS422_In_38_P		RS422_In_39_P	
21	RS422_Out_9_N	R755	RS422_Out_14_N	R769
3	RS422_Out_9_P	R754	RS422_Out_14_P	R768
4	RS422_Out_10_N	R757	RS422_Out_13_N	R767
22	RS422_Out_10_P	R756	RS422_Out_13_P	R766
5	RS422_Out_11_N	R759	RS422_Out_15_N	R771
24	RS422_Out_11_P	R758	RS422_Out_15_P	R770
20	RS422_Out_7_N	R655	RS422_Out_4_N	R645
1	RS422_Out_7_P	R654	RS422_Out_4_P	R644
7	RS422_Out_8_N	R753	RS422_Out_12_P	R764
25	RS422_Out_8_P	R752	RS422_Out_12_N	R765
2	RS422_Shield	N/A	RS422_Shield	N/A
6	RS422_Shield	N/A	RS422_Shield	N/A
23	RS422_Shield	N/A	RS422_Shield	N/A

3.2 UART

The TVS card provides 4 RS-422 UART ports. Each port is individually configurable through the USB port. All UART recieve signals are terminated with 100 ohm shunt resistors rated for 100mW. All UART transmit signals are terminated with two 45 ohm series resistors rated for 63mW each. These termination resistors may be removed or replaced with zero-ohm resistors as needed.

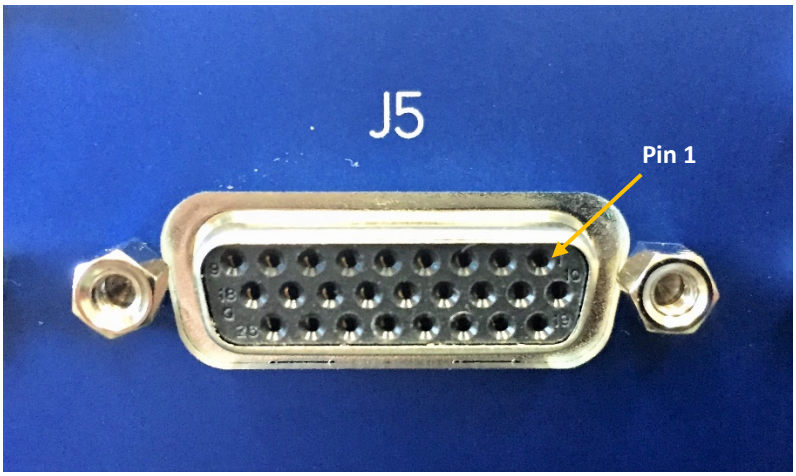


Figure 3-3 – J5

3.2.1 UART Connectors – J5

This connector contains the connections for the four UART ports according to the table below. It is a 26pin high density D-sub female connector.

Table 3-6 UART Connector – J5

Signal	Type	Connector Pin	Term. RefDes	Description
Uart1_Tx+	Output	12	R312	UART1 Transmit positive
Uart1_Tx-	Output	13	R313	UART1 Transmit negative
Uart1_Rx+	Input	17	R302	UART1 Receive positive
Uart1_Rx-	Input	16		UART1 Receive negative
Uart2_Tx+	Output	15	R314	UART2 Transmit positive
Uart2_Tx-	Output	14	R315	UART2 Transmit negative
Uart2_Rx+	Input	18	R303	UART2 Receive positive
Uart2_Rx-	Input	26		UART2 Receive negative
Uart3_Tx+	Output	5	R316	UART3 Transmit positive
Uart3_Tx-	Output	4	R317	UART3 Transmit negative
Uart3_Rx+	Input	8	R308	UART3 Receive positive

Uart3_Rx-	Input	9		UART3 Receive negative
Uart4_Tx+	Output	2	R318	UART4 Transmit positive
Uart4_Tx-	Output	3	R319	UART4 Transmit negative
Uart4_Rx+	Input	7	R309	UART4 Receive positive
Uart4_Rx-	Input	6		UART4 Receive negative
Ground	GND	1	NA	UART Signal Return
Ground	GND	22	NA	UART Signal Return
Ground	GND	24	NA	UART Signal Return
Ground	GND	25	NA	UART Signal Return

3.3 SpaceWire

The TVS card contains 4 independent SpaceWire links, however 6 SpaceWire connectors are provided. This arrangement allows for various configurations such as 2 redundant links and 2 non-redundant links (default), 3 redundant links, or 6 non-redundant links. Note that changing configurations requires a change to the TVS FPGA design. All SpaceWire input signals are terminated with a 100 ohm shunt resistor rated for 100mW.

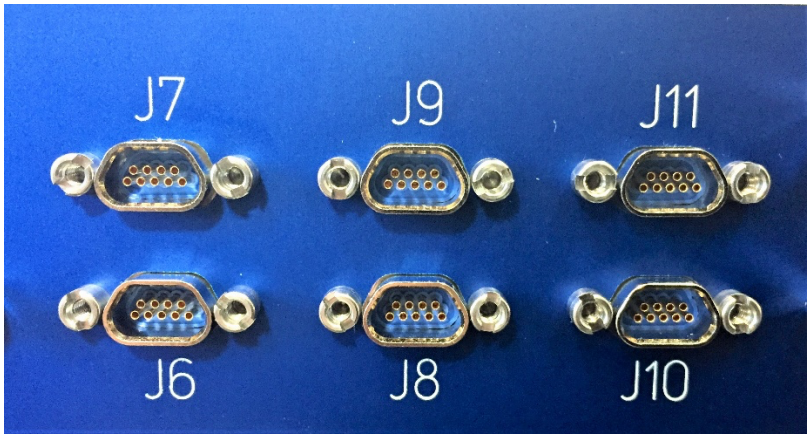


Figure 3-4 – J6 to J11

3.3.1 SpaceWire Connectors – J6 to J11

The connectors used for the SpaceWire link are GlenAir MWDM2L-9S-6K7-18B. The wiring for the connectors is per the SpaceWire ESA Standard, reference 1. The following table shows the default association between the SpaceWire links and the connectors

Table 3-7 SpaceWire Connector Assignment

SpaceWire Link	Connector	Max Speed*

Link 1	J6	196Mbps
Link 2	J7	196Mbps
Link 3 Primary	J8	155Mbps
Link 3 Redundant	J9	155Mbps
Link 4 Primary	J10	133Mbps
Link 4 Redundant	J11	133Mbps

** Based on lab testing using a 5m SpaceWire cable made with Cat5e cable. Requires configuration of XEM3010 PLL output.*

Table 3-8 SpaceWire Connectors J6 to J11

Signal	Type	J6 to J11 Connector Pin	Description
TxData+	Out	9	Transmit Data Positive
TxData-	Out	5	Transmit Data Negative
TxStrobe+	Out	8	Transmit Strobe Positive
TxStrobe-	Out	4	Transmit Strobe Negative
TxGnd	NA	3	Transmit Ground
RxData+	In	1	Receive Data Positive
RxData-	In	6	Receive Data Negative
RxStrobe+	In	2	Receive Strobe Positive
RxStrobe-	In	7	Receive Strobe Negative

Table 3-9 SpaceWire Connector J6 to J11 FPGA Pin Map on XEM3010

FPGA Pin	J6	J7	J8	J9	J10	J11
TxData	D2	C1	J6	J5	N2	M1
TxStrobe	D1	B1	K4	J4	P1	L2
RxData	G1	E1	J1	H1	K2	K5
RxStrobe	F2	E2	J2	H2	L1	K1

Table 3-10 SpaceWire Connector J6 to J11 FPGA Pin Map on XEM6310

FPGA Pin	J6	J7	J8	J9	J10	J11
TxData	C17	A17	D6	C6	D14	C14
TxStrobe	A15	A18	K18	A3	A5	E16
RxData	A10	A13	A4	A8	D7	D7
RxStrobe	C13	C15	B8	B10	D17	D8

Table 3-11 SpaceWire Connector J6 to J11 FPGA Pin Map on XEM7310

FPGA Pin	J6	J7	J8	J9	J10	J11
TxData	AA15	AB15	Y3	AA3	T5	U5
TxStrobe	AB17	Y16	R2	U2	V5	AA5
RxData	AB1	AB1	V2	Y2	AB7	R3
RxStrobe	AB16	AB16	W2	T1	AB5	AB6

3.3.2 Link Margin Testing

The SpaceWire transmit signals on J10 and J11 contain 0603 footprints for shunt termination resistors that can be used for SpaceWire link margin testing. These resistors are normally unpopulated, but by populating them, current from the TVS's LVDS driver can be shunted away from the receiving end's LVDS receiver (the DUT). Varying the value of the shunt resistor will reveal how much margin the DUT's LVDS receiver has.

Table 3-12 SpaceWire Link Margin Testing Shunt Resistor Reference Designators

Connector	Signal	Resistor
J10	TxStrobe	R284
J10	TxData	R285
J11	TxStrobe	R286
J11	TxData	R287

Table 3-13 SpaceWire Link Margins

Resistance Value (ohms)	Shunted Current (mA)	Percent margin*
2000	0.16	5%
1000	0.31	10%
667	0.44	15%
500	0.57	20%
400	0.68	25%
333	0.78	30%
286	0.88	35%
250	0.97	40%
222	1.06	45%
200	1.13	50%

** Margin is calculated as 100% * $I_{shunt}/I_{Receiver}$, assuming I_{Driver} = 3.4mA*

In addition to using the 0603 footprint on the TVS board which offers the highest fidelity of testing, one can tack-solder resistors on the pads for J6-J11. Both of these methods can stress out the pads on the TVS board after repeated soldering/desoldering. An alternative method is to make/use shunt

termination plugs in series with the SpaceWire cable. Each plug can contain a specific shunt termination resistance value.

3.4 TTL Input/Output

The TVS card provides 20 output and 8 input signals using level shifters. The part used for level shifting is the STMicroelectronics HCF40109B. Each buffer drives 4 signals and has a jumper for the V_{DD} pin of each output buffer allowing the output levels to be V_{CC} (3.3V) or V_{DC} (5V). **Note that the drive strength of the output buffer is ±1mA**.

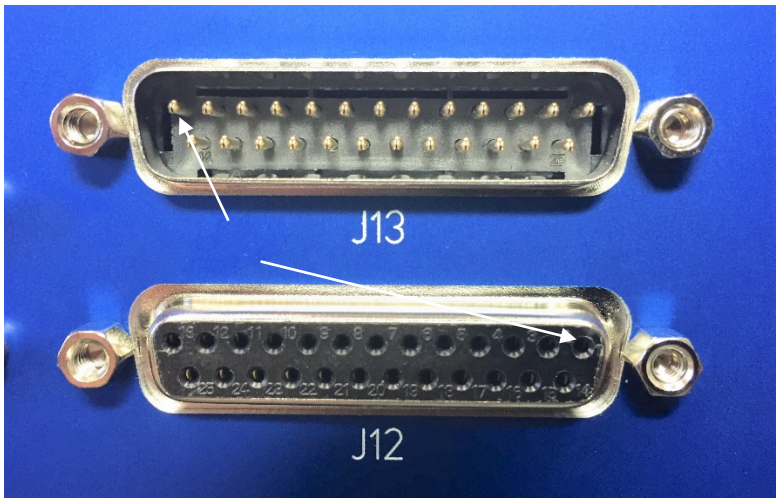


Figure 3-5 – J12 and J13

In addition, the inputs have a voltage divider stage for flexibility in reading high voltage signals (Figure 3-2 – TTL IO Voltage Divider Stage). R1 is normally open but can be replaced by a resistor or a Zener diode. The HCF40109B can handle input voltages up to 15V.

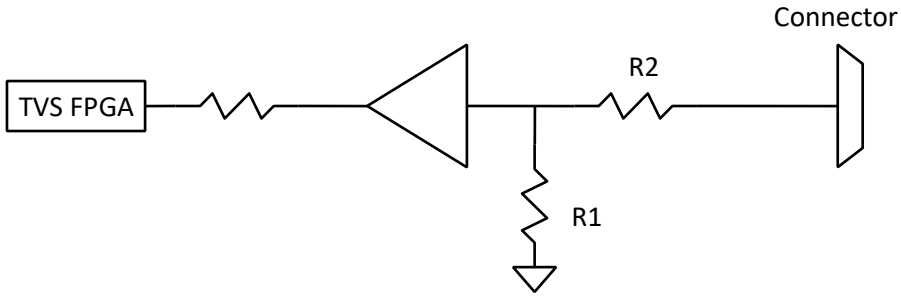


Figure 3-2 – TTL IO Voltage Divider Stage

3.4.1 xTTL Output Connector – J12

This connector contains the TTL/LVTTL output signals of the TVS card. The following table describes the connections. The connector is a 25-pin low density D-sub female connector.

Table 3-14 xTTL Output Connector – J12

Signal	Type	Connector Pin	Description	Vdd Selection Jumper
XTTLO_0	Output	15	TTL/LVTTL Output	J500
XTTLO_1	Output	14	TTL/LVTTL Output	
XTTLO_2	Output	2	TTL/LVTTL Output	
XTTLO_3	Output	1	TTL/LVTTL Output	
XTTLO_4	Output	17	TTL/LVTTL Output	J502
XTTLO_5	Output	16	TTL/LVTTL Output	
XTTLO_6	Output	4	TTL/LVTTL Output	
XTTLO_7	Output	3	TTL/LVTTL Output	
XTTLO_8	Output	6	TTL/LVTTL Output	J503
XTTLO_9	Output	19	TTL/LVTTL Output	
XTTLO_10	Output	7	TTL/LVTTL Output	
XTTLO_11	Output	18	TTL/LVTTL Output	
XTTLO_12	Output	13	TTL/LVTTL Output	J504
XTTLO_13	Output	25	TTL/LVTTL Output	
XTTLO_14	Output	12	TTL/LVTTL Output	
XTTLO_15	Output	24	TTL/LVTTL Output	
XTTLO_16	Output	8	TTL/LVTTL Output	J505
XTTLO_17	Output	21	TTL/LVTTL Output	
XTTLO_18	Output	22	TTL/LVTTL Output	
XTTLO_19	Output	9	TTL/LVTTL Output	
GND	GND	5	Ground	
GND	GND	10	Ground	
GND	GND	11	Ground	
GND	GND	20	Ground	

GND	GND	23	Ground	

3.4.2 xTTL Input Connector – J13

This connector contains the TTL/LVTTL input signals of the TVS card. The following table describes the connections. The connector is a 25-pin low density D-sub male connector.

Table 3-15 xTTL Input Connector – J13

Signal	Type	Connector Pin	Description
XTTLI_0	Input	13	TTL/LVTTL Input
XTTLI_1	Input	9	TTL/LVTTL Input
XTTLI_2	Input	10	TTL/LVTTL Input
XTTLI_3	Input	12	TTL/LVTTL Input
XTTLI_4	Input	5	TTL/LVTTL Input
XTTLI_5	Input	1	TTL/LVTTL Input
XTTLI_6	Input	2	TTL/LVTTL Input
XTTLI_7	Input	4	TTL/LVTTL Input
GND	GND	14	Ground
GND	GND	15	Ground
GND	GND	17	Ground
GND	GND	18	Ground
GND	GND	21	Ground
GND	GND	22	Ground
GND	GND	24	Ground
GND	GND	25	Ground
USB_SCL	OD	7	I2C Clock
USB_SDA	OD	20	I2C Data

3.5 Opal Kelly XEM3010

3.5.1 Board to Board Connector – J100, J101

There are two 80-pin board to board connectors from the TVS board to the XEM3010. These connectors route signals from the TVS board to the TVS FPGA according to the following table.

Table 3-16 J100 Pinout

Connector Pin	Signal	Type	FPGA Pin	Connector Pin	Signal	Type	FPGA Pin
1	Vdc	Pwr	N/A	41	J11_RxData	In	K5
2	Gnd	Pwr	N/A	42	XTTLO_11	Out	L5
3	Vdc	Pwr	N/A	43	J8_TxStrobe	Out	K4
4	NC			44	XTTLO_9	Out	L6
5	Vdc	Pwr	N/A	45	J8_TxData	Out	J6
6	NC			46	XTTLO_8	Out	K6
7	NC			47	J9_TxData	Out	J5
8	NC			48	XTTLO_6	Out	H6
9	Vcc	Pwr	N/A	49	J9_TxStrobe	Out	J4
10	USB_SCL	OD	U13	50	XTTLO_7	Out	H5
11	Vcc	Pwr	N/A	51	J8_RxData	In	J1
12	USB_SDA	OD		52	XTTLO_5	Out	G5
13	Vcc	Pwr	N/A	53	J8_RxStrobe	In	J2
14	Gnd	Pwr	N/A	54	XTTLO_4	Out	F5
15	XTTLI_5	In	U1	55	Gnd	Pwr	N/A
16	XTTLI_0	In	T3	56	NC		
17	XTTLI_3	In	T1	57	J9_RxData	In	H1
18	XTTLI_1	In	T2	58	XTTLO_2	Out	H3
19	XTTLI_2	In	R2	59	J9_RxStrobe	In	H2
20	XTTLI_4	In	R3	60	XTTLO_3	Out	H4
21	XTTLI_7	In	R1	61	J6_RxData	In	G1
22	XTTLO_18	Out	P4	62	XTTLO_1	Out	G3
23	XTTLI_6	In	P2	63	J6_RxStrobe	In	F2
24	XTTLO_19	Out	P3	64	XTTLO_0	Out	G4
25	J10_TxStrobe	Out	P1	65	J7_RxData	In	E1
26	XTTLO_17	Out	N4	66	Uart1_Rx	In	F4
27	J10_TxData	Out	N2	67	J7_RxStrobe	In	E2
28	XTTLO_16	Out	M4	68	Uart4_Rx	In	E3
29	J11_TxData	Out	M1	69	J6_TxStrobe	Out	D1
30	XTTLO_14	Out	M3	70	Uart3_Tx	Out	E4
31	J11_TxStrobe	Out	L2	71	J6_TxData	Out	D2
32	XTTLO_15	Out	L4	72	Uart2_Tx	Out	D3
33	J10_RxStrobe	In	L1	73	J7_TxData	Out	C1
34	XTTLO_13	Out	L3	74	Uart1_Tx	Out	C2
35	Gnd	Pwr	N/A	75	J7_TxStrobe	Out	B1
36	NC			76	Uart4_Tx	Out	C3
37	J10_RxData	In	K2	77	NC		
38	XTTLO_12	Out	N5	78	Gnd	Pwr	N/A
39	J11_RxStrobe	In	K1	79	NC		
40	XTTLO_10	Out	M5	80	Gnd	Pwr	N/A

Table 3-17 J101 Pinout

Connector Pin	Signal	Type	FPGA Pin	Connector Pin	Signal	Type	FPGA Pin
1	Gnd	Pwr	N/A	41	RS422 Out 14	Out	K13
2	Vcc	Pwr	N/A	42	RS422 In 35	In	L14
3	NC			43	RS422 Out 15	Out	K14
4	Vcc	Pwr	N/A	44	RS422 In 34	In	L13
5	NC			45	RS422 In 0	In	K15
6	Vcc	Pwr	N/A	46	RS422 In 1	In	J13
7	NC			47	RS422 In 3	In	J14
8	NC			48	RS422 In 2	In	H13
9	NC			49	RS422 In 6	In	J15
10	NC			50	RS422 In 5	In	H14
11	NC			51	RS422 In 7	In	G14
12	NC			52	RS422 In 4	In	J18
13	Gnd	Pwr	N/A	53	RS422 Out 1	Out	F14
14	Gnd	Pwr	N/A	54	RS422 Out 5	Out	J17
15	RS422 In 24	In	T16	55	NC		
16	RS422 In 37	In	U18	56	Gnd	Pwr	N/A
17	RS422 In 25	In	T17	57	RS422 Out 0	Out	H16
18	RS422 In 36	In	T18	58	RS422 Out 4	Out	H18
19	RS422 In 26	In	R16	59	RS422 Out 2	Out	H15
20	RS422 In 39	In	R17	60	RS422 Out 6	Out	H17
21	RS422 In 27	In	P15	61	RS422 Out 3	Out	G16
22	RS422 In 38	In	R18	62	RS422 Out 7	Out	G18
23	RS422 In 9	In	P16	63	RS422 In 29	In	G15
24	RS422 In 10	In	P17	64	RS422 In 17	In	F17
25	RS422 In 8	In	N15	65	RS422 Out 8	Out	F15
26	RS422 In 11	In	P18	66	RS422 In 16	In	E18
27	RS422 In 22	In	M15	67	RS422 Out 9	Out	E16
28	RS422 In 23	In	N17	68	RS422 In 28	In	E17
29	RS422 In 21	In	M16	69	RS422 Out 10	Out	E15
30	RS422 In 33	In	M18	70	RS422 In 18	In	D18
31	RS422 In 20	In	L15	71	RS422 Out 11	Out	D16
32	RS422 In 32	In	L17	72	RS422 In 19	In	D17
33	RS422 In 13	In	L16	73	Uart2 Rx	In	C17
34	RS422 In 12	In	L18	74	RS422 In 30	In	C18
35	NC			75	Uart3 Rx	In	C16
36	Gnd	Pwr	N/A	76	RS422 In 31	In	B18
37	RS422 Out 12	Out	N14	77	NC		
38	RS422 In 14	In	K17	78	Gnd	Pwr	N/A
39	RS422 Out 13	Out	M14	79	NC		
40	RS422 In 15	In	K18	80	Gnd	Pwr	N/A

3.5.2 Configuration

The XEM3010 must be configured for use with the TVS card as follows:

1. FB2, 3, 4 and 5 must all be installed.
2. If on-board Xilinx Configuration PROM is used, J1(on top side) must be open, otherwise J1should be closed to allow the Xilinx FPGA to be configured through the USB port.
3. If on-board Xilinx Configuration PROM is used, J2 (on top side) can be closed to allow S2 (pushbutton switch) to force the Xilinx FPGA to re-load its configuration from PROM. Leave J2 open if Xilinx FPGA is to be programmed through the USB port.
4. J3 (solder jumper on bottom side) must be open when powering the TVS with an external power supply. J3 must be closed when powering the TVS through USB power. Note that 5V power may be applied either at the power jack (J16) on the XEM3010 or J15 of the TVS board when J3 is open. Note that use of J16 is not recommended. See section 3.8.3 for more details.

3.6 Opal Kelly XEM6310

3.6.1 Board to Board Connector – JP1, JP2

There are two 80-pin board to board connectors from the TVS board to the XEM6310. These connectors route signals from the TVS board to the TVS FPGA according to the following table.

Table 3-18 JP1 Pinout

Connector Pin	Signal	Type	FPGA Pin	Connector Pin	Signal	Type	FPGA Pin
1	Vdc	Pwr	N/A	41	J11_RxData	In	L17
2	Gnd	Pwr	N/A	42	XTTLO_11	Out	D11
3	Vdc	Pwr	N/A	43	J8_TxStrobe	Out	K18
4	NC			44	XTTLO_9	Out	C12
5	Vdc	Pwr	N/A	45	J8_TxData	Out	D6
6	NC			46	XTTLO_8	Out	D15
7	NC			47	J9_TxData	Out	C6
8	NC			48	XTTLO_6	Out	C16
9	Vcc	Pwr	N/A	49	J9_TxStrobe	Out	A3
10	USB_SCL	OD	U13	50	XTTLO_7	Out	B6
11	Vcc	Pwr	N/A	51	J8_RxData	In	A4
12	NC			52	XTTLO_5	Out	A6
13	Vcc	Pwr	N/A	53	J8_RxStrobe	In	B8
14	Gnd	Pwr	N/A	54	XTTLO_4	Out	C7
15	XTTLI_5	In	W20	55	Gnd	Pwr	N/A
16	XTTLI_0	In	T19	56	NC		
17	XTTLI_3	In	W22	57	J9_RxData	In	A8
18	XTTLI_1	In	T20	58	XTTLO_2	Out	A7
19	XTTLI_2	In	U19	59	J9_RxStrobe	In	B10
20	XTTLI_4	In	P17	60	XTTLO_3	Out	C9
21	XTTLI_7	In	V20	61	J6_RxData	In	A10
22	XTTLO_18	Out	N16	62	XTTLO_1	Out	A9
23	XTTLI_6	In	C5	63	J6_RxStrobe	In	C13
24	XTTLO_19	Out	M17	64	XTTLO_0	Out	B12
25	J10_TxStrobe	Out	A5	65	J7_RxData	In	A13
26	XTTLO_17	Out	M18	66	Uart1_Rx	In	A12
27	J10_TxData	Out	D14	67	J7_RxStrobe	In	C15
28	XTTLO_16	Out	P18	68	Uart4_Rx	In	B14
29	J11_TxData	Out	C14	69	J6_TxStrobe	Out	A15
30	XTTLO_14	Out	R19	70	Uart3_Tx	Out	A14
31	J11_TxStrobe	Out	E16	71	J6_TxData	Out	C17
32	XTTLO_15	Out	D9	72	Uart2_Tx	Out	B16
33	J10_RxStrobe	In	D17	73	J7_TxData	Out	A17
34	XTTLO_13	Out	C8	74	Uart1_Tx	Out	A16
35	Gnd	Pwr	N/A	75	J7_TxStrobe	Out	A18
36	NC			76	Uart4_Tx	Out	B18
37	J10_RxData	In	D7	77	NC		
38	XTTLO_12	Out	D10	78	Gnd	Pwr	N/A
39	J11_RxStrobe	In	D8	79	NC		
40	XTTLO_10	Out	C10	80	Gnd	Pwr	N/A

Table 3-19 JP2 Pinout

Connector Pin	Signal	Type	FPGA Pin	Connector Pin	Signal	Type	FPGA Pin
1	Gnd	Pwr	N/A	41	RS422 Out 14	Out	T21
2	Vcc	Pwr	N/A	42	RS422 In 35	In	U20
3	NC			43	RS422 Out 15	Out	T22
4	Vcc	Pwr	N/A	44	RS422 In 34	In	U22
5	NC			45	RS422 In 0	In	P21
6	Vcc	Pwr	N/A	46	RS422 In 1	In	R20
7	NC			47	RS422 In 3	In	P22
8	NC			48	RS422 In 2	In	R22
9	NC			49	RS422 In 6	In	M21
10	NC			50	RS422 In 5	In	N20
11	NC			51	RS422 In 7	In	M22
12	NC			52	RS422 In 4	In	N22
13	Gnd	Pwr	N/A	53	RS422 Out 1	Out	L20
14	Gnd	Pwr	N/A	54	RS422 Out 5	Out	M20
15	RS422 In 24	In	G16	55	NC		
16	RS422 In 37	In	G19	56	Gnd	Pwr	N/A
17	RS422 In 25	In	G17	57	RS422 Out 0	Out	L22
18	RS422 In 36	In	F20	58	RS422 Out 4	Out	L19
19	RS422 In 26	In	H19	59	RS422 Out 2	Out	H21
20	RS422 In 39	In	H20	60	RS422 Out 6	Out	K21
21	RS422 In 27	In	H18	61	RS422 Out 3	Out	H22
22	RS422 In 38	In	J19	62	RS422 Out 7	Out	K22
23	RS422 In 9	In	F16	63	RS422 In 29	In	F21
24	RS422 In 10	In	D19	64	RS422 In 17	In	G20
25	RS422 In 8	In	F17	65	RS422 Out 8	Out	F22
26	RS422 In 11	In	D20	66	RS422 In 16	In	G22
27	RS422 In 22	In	J17	67	RS422 Out 9	Out	D21
28	RS422 In 23	In	F18	68	RS422 In 28	In	E20
29	RS422 In 21	In	K17	69	RS422 Out 10	Out	D22
30	RS422 In 33	In	F19	70	RS422 In 18	In	E22
31	RS422 In 20	In	K16	71	RS422 Out 11	Out	B21
32	RS422 In 32	In	M16	72	RS422 In 19	In	C20
33	RS422 In 13	In	J16	73	Uart2 Rx	In	B22
34	RS422 In 12	In	L15	74	RS422 In 30	In	C22
35	NC			75	Uart3 Rx	In	A21
36	Gnd	Pwr	N/A	76	RS422 In 31	In	A20
37	RS422 Out 12	Out	V21	77	NC		J20
38	RS422 In 14	In	K20	78	Gnd	Pwr	N/A
39	RS422 Out 13	Out	V22	79	NC		
40	RS422 In 15	In	K19	80	Gnd	Pwr	N/A

3.7 Opal Kelly XEM7310

3.7.1 Board to Board Connector – MC1, MC2

There are two 80-pin board to board connectors from the TVS board to the XEM7310. These connectors route signals from the TVS board to the TVS FPGA according to the following table.

Table 3-20 MC1 Pinout

Connector Pin	Signal	Type	FPGA Pin	Connector Pin	Signal	Type	FPGA Pin
1	Vdc	Pwr	N/A	41	J11_RxData	In	R3
2	Gnd	Pwr	N/A	42	XTTLO_11	Out	Y6
3	Vdc	Pwr	N/A	43	J8_TxStrobe	Out	R2
4	NC			44	XTTLO_9	Out	AA6
5	Vdc	Pwr	N/A	45	J8_TxData	Out	Y3
6	NC			46	XTTLO_8	Out	AA8
7	NC			47	J9_TxData	Out	AA3
8	NC			48	XTTLO_6	Out	AB8
9	Vcc	Pwr	N/A	49	J9_TxStrobe	Out	U2
10	USB_SCL	OD	U13	50	XTTLO_7	Out	U3
11	Vcc	Pwr	N/A	51	J8_RxData	In	V2
12	USB_SDA	OD		52	XTTLO_5	Out	V3
13	Vcc	Pwr	N/A	53	J8_RxStrobe	In	W2
14	Gnd	Pwr	N/A	54	XTTLO_4	Out	W1
15	XTTLI_5	In	W9	55	Gnd	Pwr	N/A
16	XTTLI_0	In	V9	56	NC		
17	XTTLI_3	In	Y9	57	J9_RxData	In	Y2
18	XTTLI_1	In	V8	58	XTTLO_2	Out	Y1
19	XTTLI_2	In	R6	59	J9_RxStrobe	In	T1
20	XTTLI_4	In	V7	60	XTTLO_3	Out	AB3
21	XTTLI_7	In	T6	61	J6_RxData	In	U1
22	XTTLO_18	Out	W7	62	XTTLO_1	Out	AB2
23	XTTLI_6	In	U6	63	J6_RxStrobe	In	AA1
24	XTTLO_19	Out	Y8	64	XTTLO_0	Out	Y13
25	J10_TxStrobe	Out	V5	65	J7_RxData	In	AB1
26	XTTLO_17	Out	Y7	66	Uart1_Rx	In	AA14
27	J10_TxData	Out	T5	67	J7_RxStrobe	In	AB16
28	XTTLO_16	Out	W6	68	Uart4_Rx	In	AA13
29	J11_TxData	Out	U5	69	J6_TxStrobe	Out	AB17
30	XTTLO_14	Out	W5	70	Uart3_Tx	Out	AB13
31	J11_TxStrobe	Out	AA5	71	J6_TxData	Out	AA15
32	XTTLO_15	Out	R4	72	Uart2_Tx	Out	W15
33	J10_RxStrobe	In	AB5	73	J7_TxData	Out	AB15
34	XTTLO_13	Out	T4	74	Uart1_Tx	Out	W16
35	Gnd	Pwr	N/A	75	J7_TxStrobe	Out	Y16
36	NC			76	Uart4_Tx	Out	AA16
37	J10_RxData	In	AB7	77	NC		
38	XTTLO_12	Out	Y4	78	Gnd	Pwr	N/A
39	J11_RxStrobe	In	AB6	79	NC		
40	XTTLO_10	Out	AA4	80	Gnd	Pwr	N/A

Table 3-21 MC2 Pinout

Connector Pin	Signal	Type	FPGA Pin	Connector Pin	Signal	Type	FPGA Pin
1	Gnd	Pwr	N/A	41	RS422 Out 14	Out	K1
2	Vcc	Pwr	N/A	42	RS422 In 35	In	J5
3	NC			43	RS422 Out 15	Out	J1
4	Vcc	Pwr	N/A	44	RS422 In 34	In	H5
5	NC			45	RS422 In 0	In	H3
6	Vcc	Pwr	N/A	46	RS422 In 1	In	H2
7	NC			47	RS422 In 3	In	G3
8	NC			48	RS422 In 2	In	G2
9	NC			49	RS422 In 6	In	E2
10	NC			50	RS422 In 5	In	G1
11	NC			51	RS422 In 7	In	D2
12	NC			52	RS422 In 4	In	F1
13	Gnd	Pwr	N/A	53	RS422 Out 1	Out	F3
14	Gnd	Pwr	N/A	54	RS422 Out 5	Out	E1
15	RS422 In 24	In	P5	55	NC		
16	RS422 In 37	In	P6	56	Gnd	Pwr	N/A
17	RS422 In 25	In	P4	57	RS422 Out 0	Out	E3
18	RS422 In 36	In	N5	58	RS422 Out 4	Out	D1
19	RS422 In 26	In	N4	59	RS422 Out 2	Out	B1
20	RS422 In 39	In	P2	60	RS422 Out 6	Out	C2
21	RS422 In 27	In	N3	61	RS422 Out 3	Out	A1
22	RS422 In 38	In	N2	62	RS422 Out 7	Out	B2
23	RS422 In 9	In	L5	63	RS422 In 29	In	K4
24	RS422 In 10	In	R1	64	RS422 In 17	In	U15
25	RS422 In 8	In	L4	65	RS422 Out 8	Out	J4
26	RS422 In 11	In	P1	66	RS422 In 16	In	V15
27	RS422 In 22	In	M6	67	RS422 Out 9	Out	T16
28	RS422 In 23	In	M2	68	RS422 In 28	In	T14
29	RS422 In 21	In	M5	69	RS422 Out 10	Out	U16
30	RS422 In 33	In	M2	70	RS422 In 18	In	T15
31	RS422 In 20	In	M1	71	RS422 Out 11	Out	V13
32	RS422 In 32	In	K6	72	RS422 In 19	In	W14
33	RS422 In 13	In	L1	73	Uart2 Rx	In	V14
34	RS422 In 12	In	J6	74	RS422 In 30	In	Y14
35	NC			75	Uart3 Rx	In	Y11
36	Gnd	Pwr	N/A	76	RS422 In 31	In	Y12
37	RS422 Out 12	Out	K2	77	NC		
38	RS422 In 14	In	L3	78	Gnd	Pwr	N/A
39	RS422 Out 13	Out	J2	79	NC		
40	RS422 In 15	In	K3	80	Gnd	Pwr	N/A

3.8 Power

The TVS card can be powered in two ways, the USB connector on the Opal Kelly XEM boards or the external power connectors, J15 and J16. The *Power Source* switch determines which power source will be used to power the TVS. Each power source has a red LED to indicate the presence of power. The *On/Off* switch determines if power is applied to the TVS and Opal Kelly board. The 3.3V LED indicates the status of the 3.3V output of the Opal Kelly board.

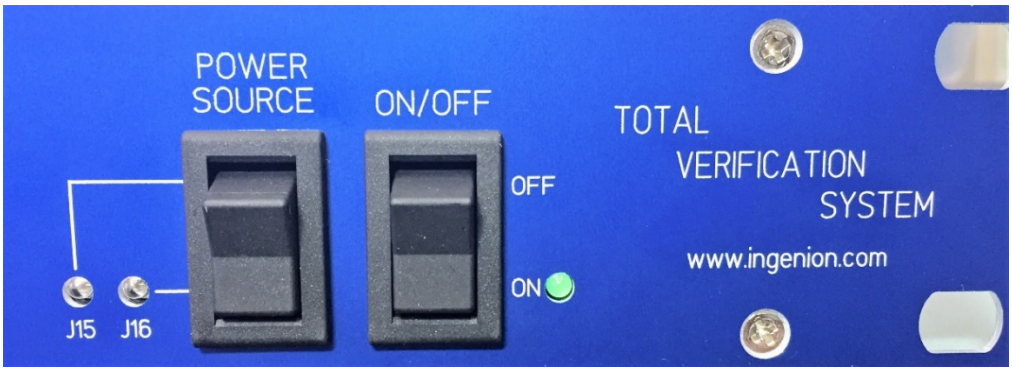


Figure 3-6 – TVS Power

3.8.1 USB Power for XEM Boards

The USB connector on the Opal Kelly XEM boards receive 5V as per the USB standard. The Opal Kelly cards regulate the 5V down to 3.3V and 1.2V. The 3.3V supply is used by the TVS card's LVDS/RS422 drivers/receivers, and the Vcc input of the level shifters. When the TVS is connected to engineering test units, ETUs, breadboards, or development units, using USB power is convenient and acceptable. Keep in mind, however, that the USB standard limits the 5V power that a host or hub must provide to either 100mA (low power) or 500mA (high power). Refer to the specifications of the USB host/hub that the TVS is connected to for more details. If the TVS is expected to draw more power than the USB host/hub can provide, the external power source should be selected.

3.8.2 External Power – J15

When the TVS card is connected to space flight hardware, the external power connector should be used to power the TVS card with a regulated external supply that is in calibration. The power supply should be set to 5V $\pm$ 0.5V. Set the overcurrent protection appropriately (this varies based on TVS FPGA utilization and frequency). Set the overvoltage protection to 5.6V.

Figure 3-6.2 – J15 Power Supply

The following table describes the external power connector. The connector is a 9-pin low density D-sub male connector.

Table 3-22 External Power Connector – J15

Signal	Connector Pin	Description
Vdc	1	+5V
Vdc	2	+5V
Vdc	6	+5V
Vdc	7	+5V
Ground	4	+5V Return
Ground	5	+5V Return
Ground	8	+5V Return
Ground	9	+5V Return

** Unlisted connector pins are no connects*

3.8.3 External Power – J16

All the XEM boards have a DC power jack input which is labeled J16 on the TVS. A 5V wall adapter can be used to power the TVS using J16. The proper wall adapter for the XEM3010 can be purchased from Opal Kelly (part number PSS050-25). The XEM6310 and XEM7310 wall adapters can be purchased CUI, Inc (part number PJ-102AH).

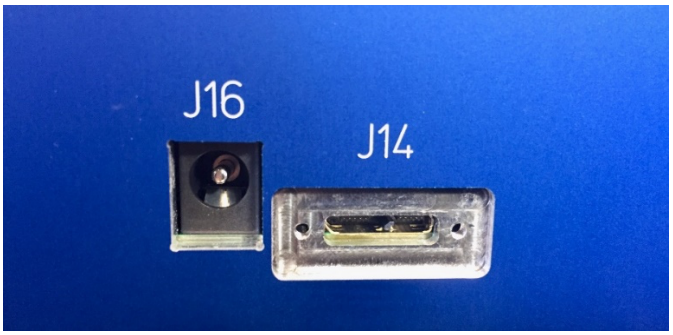


Figure 3-6.3 – J16 and J14

4. Appendix A - Loopback Plugs

Optional loopback plugs can be purchased to fully test the functionality of the TVS. This loopback plugs can be used with the free software located on the Ingenion website. Testing a TVS before use is important to detect any issues caused during production or shipping.

4.1 LP1

Loopback 1 is used to test the functionality of J1 and J2 ports on the TVS. Loopback 1 has three output ports LP1A, LP1B and LP1C. Each must be plugged in to fully test J1 and J2. Loopback 1 is shown in the figures below.

Figure 4-1 – LP1

4.2 LP2

Loopback 2 is used to test the functionality of J3 and J4 ports on the TVS. Loopback 2 has three output ports LP2A, LP2B and LP2C. Each must be plugged in to fully test J3 and J4. Loopback 2 is shown in the figures below.

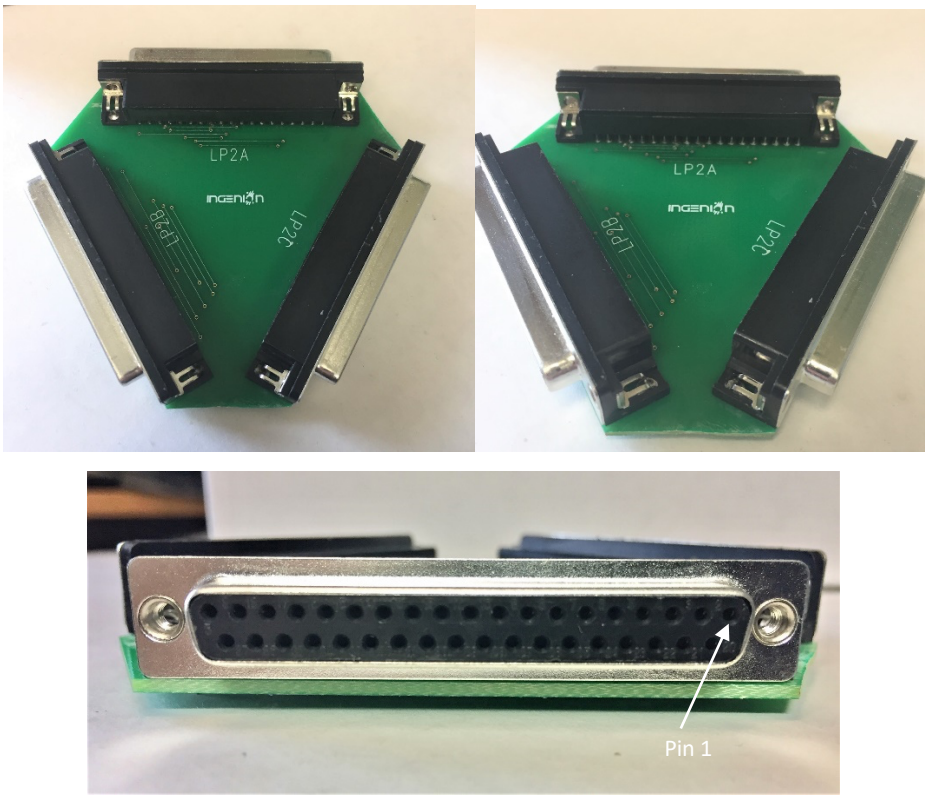


Figure 4-2 – LP2

4.3 LP3

Loopback 3 tests the functionality of port J5. Loopback 3 is shown below.

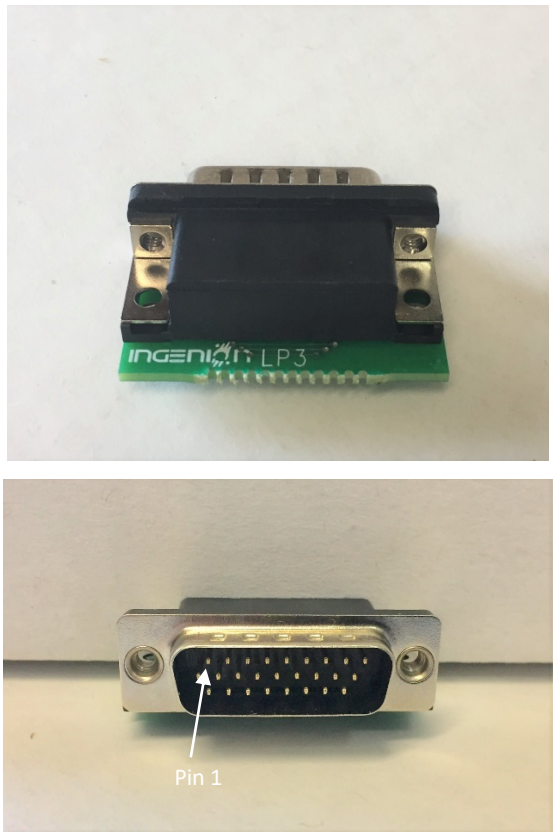


Figure 4-3 – LP3

4.4 LP4

Loopback 4 tests the functionality of ports J6 to J11. Loopback 4 must be plugged in to each port individually for testing. Loopback 4 is shown below.

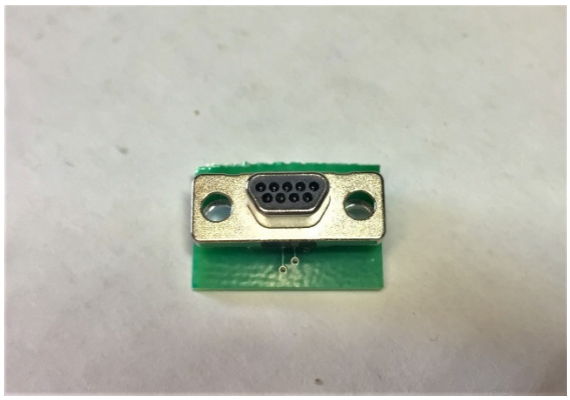


Figure 4-4 – LP4

4.5 LC5

Loopback 5 is used to test the functionality of J12 and J13 ports on the TVS. Loopback 5 has three input and output ports LC5A, LC5B and LC5C. Each must be plugged in to fully test J3 and J4 with both male and female connectors in place. Loopback 5 is shown in the figures below.

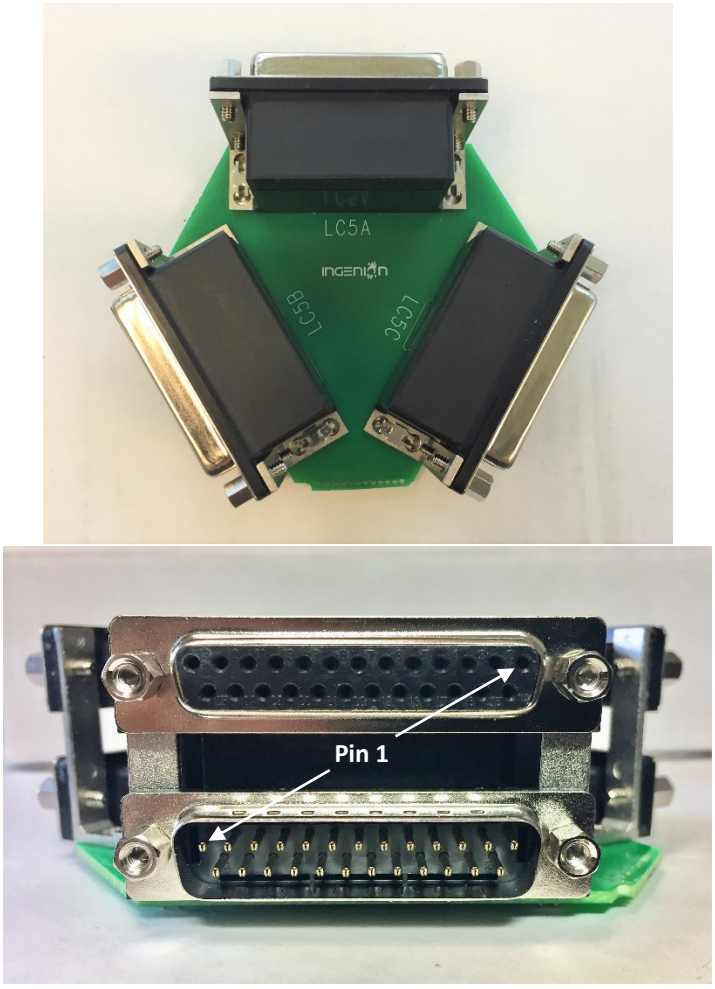


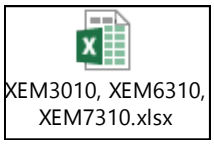
Figure 4-5 – LP5

5. Appendix B - FPGA Pinout Attachments

The following spreadsheets offer pinout planning for TVS interfaces with user-designs as well as planning for each FPGA that can come with a TVS.

Note: To open the following excel spreadsheets, please download the Word Document version of this document.

The excel spreadsheet attached below has a table and a comparison of pins from each FPGA in a TVS: XEM3010, XEM6310, and XEM7310.



The spreadsheet attached below has the IO planning for each TVS interface that outlines the IO standard and signal name and direction.